CLAIMS:

1. A memory device comprising:

an array of memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;

a mode register; and

address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register.

2. The memory device of claim 1 wherein the addressable banks can be configured as either four or eight banks.

3. The memory device of claim 1 wherein the address circuitry selectively routes address signal to either a row decoder or a bank decoder in response to the mode register.

4. A dynamic random access memory comprising:

an array of X memory cells;

a mode register; and

address circuitry coupled to the mode register to configure the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array.

5. The dynamic random access memory of claim 4 wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

6. The dynamic random access memory of claim 4 wherein the address circuitry comprises column, row and bank address decoders.

7. The dynamic random access memory of claim 6 wherein the address circuitry routes a selected address input signal to either the row or bank decoder in response to the mode register.

8. The dynamic random access memory of claim 7 wherein the address circuitry comprises a multiplex circuit.

9. A synchronous dynamic random access memory (SDRAM) comprising:

an array of X memory cells;

a mode register;

a column address decoder;

a row address decoder;

a bank address decoder; and

address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored in the mode register.

10. The SDRAM of claim 9 wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

11. The SDRAM of claim 10 wherein X = 4 and Z = 8.

12. A method of operating a memory device comprising:

programming a mode register of the memory device; and

adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array.

13. The method of claim 12 wherein the address circuitry routes an externally provided address signal to either a bank address decoder or a row address decoder.

14. The method of claim 12 wherein the memory device comprises X rows, Y columns and Z banks, where the array comprises X*Y*Z memory cells.

15. The method of claim 14 where the Z banks are configurable to 2, 4, 8 or 16 banks.

16. A method of operating a memory system comprising:

outputting mode register data from a processor to a memory device, wherein the mode register data contains bank count data;

programming a mode register of the memory device with the mode register data; and

adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array using the bank count data.

17. The method of claim 16 wherein the mode register data comprises one bit of data.

18. The method of claim 16 wherein the address circuitry routes externally address signals provided by the processor to either a bank address decoder or a row address decoder of the memory device.

19. A synchronous dynamic random access memory (SDRAM) comprising:

an array of X memory cells;

at least one external input connection to receive a configuration signal;

logic circuitry coupled to the at least one external input connection;

a column address decoder;

a row address decoder;

a bank address decoder; and

address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to the logic circuitry.

20. The SDRAM of claim 19 wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

21. The SDRAM of claim 20 wherein X = 4 and Z = 8.

22. The SDRAM of claim 19 wherein the at least one external input connection comprises two input connections to receive a two-bit configuration signal.